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Tina Kayanauch

(Depositor's name)

May 2, 2005

(Date)

APPLICATION NO. PILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/619.711	07/14/2003	Jason Cheng	M-9559-2P US	7093	

TITLE OF INVENTION: PROGRAMMABLE LOGIC DEVICE WITH ENHANCED WIDE INPUT PRODUCT TERM CASCADING

APPLN. TYPE	SMALL ENTITY	ISSUE FE	Œ	PUBLICATION FEE	TOTAL PER(S) DOR	DATEDUE
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CHO, JAME	S HYONCHOL	2819		326-041000		
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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Chan-Chi Jason Cheng; Cyrus Tsui; Satwant Singh; Albert Chan; Ju

Shen; Clement Lee

Assignee:

Lattice Semiconductor Corporation

Title:

Programmable Logic Device With Enhanced Wide Input Product Term

Cascading

Serial No.:

10/619,711

Filing Date:

7/14/2003

Examiner:

Cho, James Hyonchol

Group Art Unit:

2819

Docket No.:

M-9559-2P US

Confirmation

7093

No.

Irvine, California May 2, 2005

Fax No.: 1-703-746-4000

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2. Fee Address "Indication Form" (1 page)

Dated: May 2, 2005

Tina Kayananoh

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Serial No. 10/619,711



T; 949-752-7040 F; 949-752-7049

## MacPherson Kwok Chen & Heid LLP

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